IN THE UNITED STATES DISTRICT COURT

FOR THE NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

Acer, Inc.,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

HTC Corp.,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

Barco NV,

Plaintiff,

v.

Technology Properties Ltd, et al.,

Defendants.
_____/

NO. C 08-00877 JW
NO. C 08-00882 JW
NO. C 08-05398 JW

FIRST CLAIM CONSTRUCTION ORDER

I. INTRODUCTION

Technology Properties Limited, Patriot Scientific Corporation and Alliacense, Ltd. (collectively, "Defendants") own a group of five patents known as the Moore Microprocessor

Portfolio patents.[1] Plaintiffs Acer, Inc.,[2] HTC Corp.[3] and Barco, N.V.[4] each filed lawsuits seeking a judicial declaration that the Patents-in-Suit are either invalid or are not infringed. Defendants filed counterclaims for infringement of the Patents-in-Suit. In due course, the actions were related and consolidated.[5]

On January 27, 2012, the Court conducted a hearing in accordance with Markman v. Westview Instruments, Inc.,[6] to construe language of the asserted claims over which there is a dispute. At the hearing, in addition to the normal intrinsic evidence, the parties relied upon a prior

---

[1] The five Patents-in-Suit are U.S. Patent Nos. 5,809,336 ("the '336 Patent"), 5,784,584 ("the '584 Patent"), 5,440,749 ("the '749 Patent"), 6,598,148 ("the '148 Patent") and 5,530,890 ("the '890 Patent").

[2] The first of these now-consolidated actions was filed on February 8, 2008. Acer filed suit against Defendants seeking a judicial declaration that the '336 Patent, the '584 Patent and the '749 Patent are invalid or are not infringed by Acer. (See Docket Item No. 1 in No. C 08-00877 JW.) On November 21, 2008, Defendants counterclaimed for infringement of the '336 Patent and the '749 Patent. (See Docket Item No. 60 in No. C 08-00877 JW.) On February 9, 2009, Acer amended its complaint to add claims pertaining to the '148 Patent and the '890 Patent. (See Docket Item No. 98 in No. C 08-00877 JW.) On February 24, 2009, Defendants counterclaimed with respect to those two patents. (See Docket Item No. 99 in No. C 08-00877 JW.)

[3] On February 8, 2008, HTC also filed suit seeking a judicial declaration that the '336 Patent, the '584 Patent, the '749 Patent and the '148 Patent are invalid or are not infringed by HTC. (See Docket Item No. 1 in No. C 08-00882 JW.) On July 10, 2008, HTC amended its complaint to add claims pertaining to the '890 Patent. (See Docket Item No. 34 in No. C 08-00882 JW.) On November 21, 2008, Defendants counterclaimed with respect to each of those patents except for the '584 Patent. (See Docket Item No. 60 in No. C 08-00882 JW.)

[4] On December 1, 2008, Barco filed suit seeking a judicial declaration that the '584 Patent, the '749 Patent and the '890 Patent are invalid or are not infringed by Barco. (See Docket Item No. 1 in No. C 08-05398 JW.) On February 17, 2009, Defendants counterclaimed for infringement with respect to the '749 Patent, the '890 Patent and the '336 Patent. (See Docket Item No. 27 in No. C 08-05398 JW.)

[5] Judge Fogel ordered the cases related. (See Docket Item No. 21 in No. C 08-00882 JW; Docket Item No. 21 in No. C 08-05398 JW.) On September 1, 2011, this matter was reassigned from Judge Fogel to Chief Judge Ware. (See Docket Item No. 291 in No. C 08-00877 JW.)

[6] 517 U.S. 370 (1996).

claim construction order by Judge T. John Ward[7] and documentary material from reexamination proceedings.[8]

This Claim Construction Order sets forth the Court's construction of disputed words and phrases tendered to the Court for construction.

II. STANDARDS AND PROCEDURES FOR CLAIM CONSTRUCTION

A. General Principles of Claim Construction

Claim construction is a matter of law, to be decided exclusively by the Court. Markman, 517 U.S. at 387. In accordance with the Patent Local Rules of the Northern District, the parties submit their joint selection of the ten disputed terms that are significant in resolving the case as well as their proposed definitions for construction. See Patent L.R. 4-3. After the Markman hearing and upon consideration of the parties' briefs, the Court issues an order construing the meaning of the disputed terms. The Court's construction becomes the legally operative meaning of the disputed terms that governs further proceedings in the case. See Chimie v. PPG Indus., Inc., 402 F.3d 1371, 1377 (Fed.

---

[7] In 2006, Defendants filed a patent infringement suit based upon three of the Patents-in-Suit in this matter–the '336 Patent, the '148 Patent and the '584 Patent–in the Eastern District of Texas. (See Order Denying Motions to Dismiss, to Transfer Venue, and to Stay at 3, Docket Item No. 47 in No. C 08-00877 JW (discussing the Texas action).) Defendants brought that action against unrelated third parties. (See id.) On June 15, 2007, Judge Ward issued a Claim Construction Order in the Texas action in which he construed some of the words and phrases from the three patents at issue in that case. See Tech. Props. Ltd. v. Matsushita Elec. Indus. Co., Ltd., 514 F. Supp. 2d 916 (E.D. Tex. 2007).

[8] As of April 30, 2009, "a total of eleven reexamination proceedings had been initiated against the [Patents-in-Suit] in the United States Patent and Trademark Office ('USPTO')." (Order Granting in part Motion to Stay at 2-3, Docket Item No. 144 in No. C 08-00877 JW.) On June 17, 2009, the Court granted in part motions to stay this action pending reexamination of several of the Patents-in-Suit. (See id.) On February 22, 2010, the Court lifted the stay. (See Docket Item No. 156 in No. C 08-00877 JW.)

The reexamination certificate for the '749 Patent was issued on June 7, 2011. (See Declaration of James C. Otteson in Support of Defendants' Opening Claim Construction Brief for the "Top Ten" Terms, hereafter, "Otteson Decl.," Ex. BB, Ex Parte Reexamination Certificate, Docket Item No. 310-6.) The reexamination of the '749 Patent resulted in amendments to Claim 1, among others. Claim 1 of the '749 Patent–which includes multiple disputed terms–was amended to include the two "wherein" clauses. (See id.)

The reexamination certificate for the '336 Patent was issued on December 15, 2009. (See Otteson Decl., Ex. DD, Ex Parte Reexamination Certificate, Docket Item No. 310-8.) The reexamination of the '336 Patent resulted in amendments to Claims 1, 6 and 10, and the addition of Claim 11, among others. (Id.)

Cir. 2005). Although greater weight should always be given to the intrinsic evidence,[9] claim construction is a fluid process in which the Court may consider a number of extrinsic sources of evidence, so long as they do not contradict the intrinsic evidence. See Vitronics Corp. v. Conceptronic, Inc., 90 F.3d 1576, 1582-83 (Fed. Cir. 1996).

B. Construction from the Viewpoint of an Ordinarily Skilled Artisan

A patent's claims define the scope of the patent: the invention that the patentee may exclude others from practicing. Phillips, 415 F.3d at 1312. The Court generally gives the patent's claims their ordinary and customary meaning. In construing the ordinary and customary meaning of a patent claim, the Court does so from the viewpoint of a person of ordinary skill in the art at the time of the invention, which is considered to be the effective filing date of the patent application. Thus, the Court seeks to construe the patent claim in accordance with what a person of ordinary skill in the art would have understood the claim to have meant at the time the patent application was filed. This inquiry forms an objective baseline from which the Court begins its claim construction. Id. at 1313.

The Court proceeds from that baseline under the premise that a person of ordinary skill in the art would interpret claim language not only in the context of the particular claim in which the language appears, but also in the context of the entire patent specification of which it is a part. Phillips, 415 F.3d at 1313. Additionally, the Court considers that a person of ordinary skill in the art would consult the rest of the intrinsic record, including any surrounding claims, the drawings and the prosecution history, if it is in evidence. Id.; see also Teleflex, Inc. v. Fisosa N. Am. Corp., 299 F.3d 1313, 1324 (Fed. Cir. 2002). In reading the intrinsic evidence, a person of ordinary skill in the art would give consideration to whether the disputed term is a term commonly used in lay language, a technical term, or a term defined by the patentee.

C. Commonly Used Terms

In some cases, disputed claim language involves a commonly understood term that is readily apparent to the Court. In such a case, the Court considers that a person of ordinary skill in the art

[9] Phillips v. AWH Corp., 415 F.3d 1303, 1324 (Fed. Cir. 2005).

would give the term its widely accepted meaning, unless a specialized definition is stated in the patent specification or was stated by the patentee during prosecution of the patent. In articulating the widely accepted meaning of such a term, the Court may consult a general purpose dictionary. Phillips, 415 F.3d at 1314.

D. Technical Terms

If a disputed term is a technical term in the field of the invention, the Court considers that one of skill in the art would give the term its ordinary and customary meaning in that technical field, unless a specialized definition is stated in the specification or during prosecution of the patent. Phillips, 415 F.3d at 1314. In arriving at this definition, the Court may consult a technical art-specific dictionary or invite the parties to present testimony from experts in the field on the ordinary and customary definition of the technical term at the time of the invention. Id.

E. Defined Terms

It is well established that a patentee is free to act as his or her own lexicographer. See, e.g., Process Control Corp. v. HydReclaim Corp., 190 F.3d 1350, 1357 (Fed. Cir. 1999). Acting as such, the patentee may use a term differently than a person of ordinary skill in the art would understand it, without the benefit of the patentee's definition. Vitronics Corp., 90 F.3d at 1582. Thus, the Court examines the claims and the intrinsic evidence to determine if the patentee used a term with a specialized meaning.

The Court regards a specialized definition of a term stated in the specification as highly persuasive of the meaning of the term as it is used in a claim. Phillips, 415 F.3d at 1316-17. However, the definition must be stated in clear words which make it apparent to the Court that the term has been defined. See id.; Vitronics Corp., 90 F.3d at 1582. If the definition is not clearly stated or cannot be reasonably inferred, the Court may decline to construe the term pending further proceedings. Statements made by the patentee in the prosecution of the patent application as to the scope of the invention may be considered when deciding the meaning of the claims. Microsoft Corp. v. Multi-Tech Systems, Inc., 357 F.3d 1340, 1349 (Fed. Cir. 2004). Accordingly, the Court

may also examine the prosecution history of the patent when considering whether to construe the claim term as having a specialized definition.

In construing claims, it is for the Court to determine the terms that require construction and those that do not. See U.S. Surgical Corp. v. Ethicon, Inc., 103 F.3d 1554, 1568 (Fed. Cir. 1997). Moreover, the Court is not required to adopt a construction of a term, even if the parties have stipulated to it. Pfizer, Inc. v. Teva Pharm. USA, Inc., 429 F.3d 1364, 1376 (Fed. Cir. 2005). Instead, the Court may arrive at its own constructions of claim terms, which may differ from the constructions proposed by the parties.

III. DISCUSSION

Pursuant to the Patent Local Rules, the parties have tendered ten terms that they have identified as significant to resolving these cases. The parties have asked the Court to consider the tendered words and phrases in a particular order. However, because the sequence in which the patents were issued might influence how a person of ordinary skill in the art would understand the patents, the Court will discuss the words and phrases in the order in which they appear in the Patents-in-Suit.[10]

A. '749 Patent

The '749 Patent is entitled: "High Performance, Low Cost Microprocessor Architecture."

Claim 1 of the '749 Patent, as allowed after reexamination, provides:[11]

> A microprocessor system, comprising a central processing unit integrated circuit, a memory external of said central processing unit integrated circuit, a bus connecting said central processing unit integrated circuit to said memory, and means connected to said bus for fetching instructions for said central processing unit integrated circuit on said bus from said memory, said means for fetching instructions being configured and connected to fetch **multiple sequential instructions** from said memory in parallel and **supply the multiple sequential instructions to said central processing unit integrated circuit during a single memory cycle**, said bus having a width at least equal to a number of bits in each of the instructions times a number of the

[10] Subject to further proceedings, the Court's construction of any particular term is presumed to apply consistently across all claims in the Patents-in-Suit in which the term appears. See, e.g., Paragon Solutions, LLC v. Timex Corp., 566 F.3d 1075, 1087 (Fed. Cir. 2009).

[11] Unless otherwise indicated, all bold typeface is added by the Court for emphasis.

> instructions fetched in parallel, said central processing unit integrated circuit including an arithmetic logic unit and **a first push down stack connected to said arithmetic logic unit**, said first push down stack including means for storing a top item connected to a first input of said arithmetic logic unit to provide the top item to the first input and means for storing a next item connected to a second input of said arithmetic logic unit to provide the next item to the second input, a remainder of said first push down stack being connected to said means for storing a next item to receive the next item from said means for storing a next item when pushed down in said push down stack, said arithmetic logic unit having an output connected to said means for storing a top item;
> wherein
> the microprocessor system comprises an **instruction register** configured to store the multiple sequential instructions and from which instructions are accessed and decoded;
> and wherein
> the means for fetching instructions being configured and connected to fetch multiple sequential instructions from said memory in parallel and supply the multiple sequential instructions to the central processing unit integrated circuit during a single memory cycle comprises supplying the multiple sequential instructions in parallel to said instruction register during the same memory cycle in which the multiple sequential instructions are fetched.

Claim 1 recites a microprocessor system. The parties have tendered for construction a number of words and phrases used in Claim 1.

1. "multiple sequential instructions"

Claim 1 recites that the system comprises, among other components, a "means for fetching"[12] that is configured to fetch "multiple sequential instructions." The parties tender for construction the phrase "multiple sequential instructions."

Upon review, the Court finds that this phrase is composed of commonly used words that have a plain and ordinary meaning. There is nothing in the claim or written description that would lead a person of ordinary skill in the art to conclude that the inventors intended to use the phrase with anything other than its plain and ordinary meaning. In particular, the Court finds that the word "multiple" would have been understood, by a person of ordinary skill in the art, to mean "two or more," while the phrase "sequential instructions" would have been understood to mean "computer

[12] For convenience, the Court will refer to this "means" as the "means for fetching limitation."

instruction in a sequential order." Therefore, at this time, the Court declines to use any different words or phrases to construe the phrase "multiple sequential instructions."

2. ". . . configured and connected to . . . supply multiple sequential instructions to central processing unit integrated circuit during a single memory cycle"

Claim 1 recites that the "means for fetching" is configured and connected to supply multiple sequential instructions to the central processing unit "during a single memory cycle." The parties request the Court to decide what, if any, effect the reexamination proceedings had on the meaning of the phrase "during a single memory cycle."[13] Specifically, the issue tendered to the Court is whether the phrase should be defined as requiring a "prefetch buffer."

During reexamination, the inventors, in referring to the phrase "during a single memory cycle," defended allowance of the claim over a prior art reference known as "Edwards" by stating the following:

> Edwards describes the way the Transputer decodes and executes instructions. As described in Edwards, see, e.g., Fig. 8, below, instructions are supplied to a one-instruction-wide instruction buffer, one at a time, and are there decoded. Fetching multiple instructions into a prefetch buffer and then supplying them one at a time is not sufficient to meet the claim limitation–the supplying of "multiple sequential instructions to a CPU during a single memory cycle."[14]

Upon review, the Court does not find that the cited statements constitute a basis for construing the language of Claim 1 to include the presence or configuration of a prefetch buffer.[15]

---

[13] (See, e.g., Plaintiffs' Consolidated Responsive Claim Construction Brief at 26-28, hereafter, "Plaintiffs' Brief," Docket Item No. 315 in No. C 08-00877 JW.)

[14] (See Declaration of Kyle Chen in Support of Plaintiffs' Consolidated Responsive Claim Construction Brief, hereafter, "Chen Decl.," Ex. 16, Amendment in Response to Non Final Office Action in Ex Parte Reexamination Proceedings at 26, Docket Item No. 316-16.)

[15] Plaintiffs cite to three additional statements made by the inventors that purportedly contain similar disavowals. (See Plaintiffs' Brief at 27-28.) However, the Court finds that none of these cited statements refer to a "prefetch buffer." Further, each cited statement expressly distinguishes the alleged invention from the prior art reference on the same basis, namely, that the instructions are supplied to the CPU "during a single memory cycle." (Id.)

Having disposed of the only issue tendered with respect to this phrase, the Court declines to further construe it.[16]

3. "push down stack connected to said arithmetic logic unit"

Claim 1 recites a central processing unit integrated circuit including an arithmetic logic unit and "a first push down stack connected to said arithmetic logic unit." The parties tender for construction the phrase "push down stack connected to said arithmetic logic unit."

As to this phrase, the Court finds that a person of ordinary skill in the art reading the '749 Patent would understand the phrase "push down stack" to mean a last-in, first-out ("LIFO") data storage structure, in which the last item placed (pushed) onto the stack is the first item removed (popped) from the stack.[17] Further, the Court finds that a person of ordinary skill in the art at the time of the invention would understand that a "push down stack" can be implemented using a dedicated top-of-stack register or a logical stack "pointer" to indicate the "top of the stack" element regardless of its location. For example, the written description discusses stack pointers 102 and 104 in Fig. 2.[18]

Finally, with respect to this phrase, the parties dispute whether the "connected to" language should be construed as "directly connected to" or "physically connected to." The claim requires that the push down stack be "connected" to the arithmetic logic unit. The Court finds that a person of

---

[16] The parties did not request the Court to construe the meaning of the phrase "during a single memory cycle."

[17] See, e.g., MODERN DICTIONARY OF ELECTRONICS 603 (7th ed. 1999) (defining a "pushdown stack" as a "circuit that operates in the reverse of a shift register," and explaining that "[w]hereas[] a shift register is a first-in first-out (FIFO) circuit, pushdown stacks are last-in, first-out (LIFO) memories. When data is requested, the stack will read the last data stored, and all other data will move one step closer to the output. Unless memory is emptied, the first data in will never be retrieved."). The same source alternatively defines a "pushdown stack" as "[e]ssentially a last-in, first-out buffer" in which, "[a]s data is added, the stack moves down with the last item, added [sic] taking the top position. Id. Thus, the "[s]tack height varies with the number of stored items, increasing or decreasing with the entering or retrieving of data. The words push (move down) and pop (retrieve the most recently stoked [sic] item) are used to describe its operation." Id.

[18] Referring to Fig. 2, the specification states: "Stack pointer 102, return stack pointer 104, mode register 106 and instruction register 108 are also connected to the internal data bus 90 by lines 110, 112, 114 and 116, respectively." (See '749 Patent, Col. 6:39-42.)

ordinary skill in the art would understand that the stack might be implemented using "pointers," which negates the need to connect the stack directly or physically to the arithmetic logic unit.[19] Therefore, the Court declines to add as a limitation that the connection must be direct or physical.

Accordingly, the Court construes the phrase "push down stack connected to said arithmetic logic unit" to mean:

a last-in-first-out data storage element connected to the arithmetic logic unit.

4. "instruction register"

Claim 1 contains two "wherein" clauses. With respect to the first "wherein" clause, the parties tender for construction the phrase "wherein the microprocessor system comprises an instruction register."[20]

In computer systems, the phrase "instruction register" has a plain and ordinary meaning, namely, a "register in a central processing unit that holds the address of the next instruction to be executed."[21] A person of ordinary skill in the art reading the written description would understand that the inventors are using the phrase with its plain and ordinary meaning:

> Instruction register 108 receives four 8-bit byte instruction words 1-4 on 32-bit internal data bus 90.

('749 Patent, Col. 7:53-55.)[22]

The parties have drawn the Court's attention to a related term that was construed by Judge Ward and that was subsequently affirmed by the Federal Circuit. Judge Ward's construction related to phrases such as "instruction groups" and "operand" in Claim 29 of the '584 Patent. See Tech.

---

[19] See MODERN DICTIONARY OF ELECTRONICS 603 (7th ed. 1999) ("In actual practice, a hardware-implemented pushdown stack is a collection of registers with a counter that serves as a pointer to indicate the most recently loaded register. Registers are unloaded in the reverse of the sequence in which they were loaded.").

[20] The Court notes that both the body of the claim and the first "wherein" clause disclose a microprocessor system *comprising* recited limitations. However, conventional claim language would have the wherein clause formatted to provide that "the microprocessor system *further* comprises . . ." to avoid any confusion between the wherein clause and the body of the claim.

[21] See MICROSOFT COMPUTER DICTIONARY 276 (5th ed. 2002).

[22] The Court notes that the phrase "8-bit byte" is unusual and appears to be redundant.

Props. Ltd., 514 F. Supp. 2d at 931-34. The claims of the '584 Patent deal specifically with an embodiment that includes "variable width operands." (See '584 Patent, Col. 16:7-26.) This particular embodiment requires all operands to be right justified in the instruction register so that the microprocessor can quickly locate the operands of variable width without the need "to specify the different operand sizes." (See '584 Patent, Col. 16:24-26.) However, unlike Claim 29 of the '584 Patent, Claim 1 of the '749 Patent does not contain such phrases. Thus, the Court does not find Judge Ward's construction pertinent.

Because the Court finds that the language of the claim has been used with its plain and ordinary meaning, the Court declines to further construe it.[23]

B. '890 Patent

Claim 11 of the '890 Patent[24] provides:

> A microprocessor, which comprises a main central processing unit and a **separate direct memory access central processing unit** in a single integrated circuit comprising said microprocessor, said main central processing unit having an arithmetic logic unit, a first push down stack with a top item register and a next item register, connected to provide inputs to said arithmetic logic unit, an output of said arithmetic logic unit being connected to said top item register, said top item register also being connected to provide inputs to an internal data bus, said internal data bus being bidirectionally connected to a loop counter, said loop counter being connected to a decrementer, said internal data bus being bidirectionally connected to a stack pointer, return stack pointer, mode register and instruction register, said stack pointer pointing into said first push down stack, said internal data bus being connected to a memory controller, to a Y register of a return push down stack, an X register and a program counter, said Y register, X register and program counter providing outputs to an internal address bus, said internal address bus providing inputs to said memory controller and to an incrementer, said

---

[23] The Court notes that in a summary of an in-person interview with the examiner issued on October 25, 1994, the examiner noted with respect to Claim 1: "operand width is variable and right adjusted." (See Chen Decl., Ex. 19, Examiner Interview Summary Record, Docket Item No. 316-20.) The statement appears to have been made in an attempt to distinguish prior art known as "Boufarah," and the Court finds that it may potentially impose a limitation on the type of operands that are to be used and the positioning of the operands in the instruction register. The Court finds that a full understanding of the meaning of this statement and the events that gave rise to it might be relevant to the present analysis. Thus, the Court finds that it would benefit from further briefing as to this issue, as discussed below.

[24] The '890 Patent and the '336 Patent were filed on the same day. However, the '890 Patent was issued earlier than the '336 Patent. (See Chen Decl. ¶¶ 2, 12 (stating that the '890 Patent was issued on June 25, 1996, while the '336 Patent was issued on September 15, 1998).)

> incrementer being connected to said internal data bus, said direct memory access central processing unit providing inputs to said memory controller, said memory controller having an address/data bus and a plurality of control lines for connection to a random access memory.

The parties tender for construction the phrase "separate direct memory access central processing unit."

Claim 11 provides two separate central[25] processing units ("CPU"): a "main" CPU and a "direct memory access" ("DMA") CPU. The Court finds that a person of ordinary skill in the art would understand "CPU" to mean a unit of a computing system that fetches, decodes, and executes programmed instructions.[26] In the written description, the inventors use the term CPU consistently with its plain and ordinary meaning.[27]

Further, the written description criticizes "[c]onventional microprocessors" that use "DMA controllers" because "some processing by the main central processing unit (CPU) of the microprocessor is required."[28] With respect to the DMA CPU, the written description states that an object of the invention is to provide a microprocessor "in which DMA does not require use of the main CPU during DMA requests and responses and which provides very rapid DMA response with predictable response times."[29]

---

[25] The parties agree that a person of ordinary skill would understand "central" processing unit to refer to a processing unit, and that the word "central" does not necessarily connote the primary processor in a particular hierarchy.

[26] See, e.g., MODERN DICTIONARY OF ELECTRONICS 107 (7th ed. 1999) (defining a CPU as "[t]hat unit of a computing system that fetches, decodes, and executes programmed instructions and maintains the status of results as the program is executed").

[27] (See, e.g., '890 Patent, Col. 8:22-24 ("The DMA CPU 72 controls itself and has the ability to fetch and execute instructions. It operates as a co-processor to the main CPU 70 (FIG. 2) for time specific processing.").)

[28] ('890 Patent, Col. 1:52-58.)

[29] ('890 Patent, Col. 2:2-5.)

Accordingly, the Court construes the term "separate direct memory access central processing unit" to mean:

> **a central processing unit that accesses memory and that fetches and executes instructions directly, separately, and independently of the main central processing unit.**

C. ‘336 Patent

1. Claim 1

Claim 1 of the ‘336 Patent provides:

> A microprocessor system, comprising
> a single integrated circuit including a central processing unit and an **entire ring oscillator variable speed system clock** in said single integrated circuit and connected to said central processing unit for clocking said central processing unit,
> said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations,
> a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit;
> an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and
> a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, wherein a clock signal of said second clock originates from a source other than said ring oscillator variable speed system clock.

The parties tender the phrase "ring oscillator" for construction.

Upon review, the Court finds that one of ordinary skill in the art would understand the phrase "ring oscillator" to mean: "interconnected electronic components comprising multiple odd numbers of inverters arranged in a loop."[30] When a voltage is applied, the ring oscillator generates signals that are used by the processing unit to regulate the timing of its operations. In contrast with a circuit

[30] The parties agree that a "ring oscillator" is "an oscillator having a multiple, odd number of inversions arranged in a loop," which is the construction arrived at by Judge Ward in the Texas action, though they disagree about whether additional limitations should be added to Judge Ward's construction of the term. (See Plaintiffs' Brief at 3; Defendants' Opening Claim Construction Brief for the "Top Ten" Terms at 16-17, Docket Item No. 310 in No. C 08-00877 JW.)

that receives its timing signal from an external clock, a person of ordinary skill in the art reading the patent would understand that Claim 1 claims a "single integrated circuit," fabricated so as to include a "ring oscillator."

At issue is whether the phrase "ring oscillator" should be given a specialized meaning based on statements made by the inventors during reexamination of Claims 4 and 8 of the '148 Patent.[31]

Claim 4 of the '148 Patent claims in pertinent part:

> A microprocessor integrated circuit comprising . . . a ring oscillator having a variable output frequency, wherein the ring oscillator provides a system clock to the processing unit, the ring oscillator disposed on said integrated circuit substrate.

Claim 8 of the '148 Patent has a similarly worded limitation.

During reexamination, the examiner reviewed the allowance of Claims 4 and 8 over U.S. Patent No. 4,689,581 ("Talbot"). The Talbot Patent, which is entitled "Integrated Circuit Phase Locked Loop Timing Apparatus," claims:

> an integrated circuit device . . . and a timing apparatus . . . formed on a common single chip, said timing apparatus comprising a phase locked loop [comprising, *inter alia*] a voltage controlled oscillator arranged to be controlled by [a] voltage signal to produce [an] output timing signal at its output.

(Talbot, Col. 10:48-11:9.)

Preliminarily, the examiner rejected Claims 4 and 8 of the '148 Patent as unpatentable over Talbot. During the course of reexamination proceedings, the examiner conducted an interview with the patent owner and discussed whether Claims 4 and 8 were allowable over Talbot.[32] Afterward,

---

[31] Because the '148 Patent shares the same specification with the '336 Patent and is directly related to the other three Patents-in-Suit, the Court finds that any representation regarding similar terms made by the inventors during the prosecution of the '148 Patent is relevant to its consideration and construction of the terms in the '336 Patent. See Microsoft Corp. v. Multi-Tech Sys., Inc., 357 F.3d 1340, 1350 (Fed. Cir. 2004) ("Any statement of the patentee in the prosecution of a related application as to the scope of the invention would be relevant to claim construction.").

[32] (See Otteson Decl., Ex. X, Ex Parte Reexamination Interview Summary, Docket Item No. 310-2.)

the examiner prepared and sent to the patent owner an "Interview Summary."[33] Specifically, with respect to the discussion of Talbot, the examiner wrote:

> Continuing, the patent owner further argued that the reference of Talbot does not teach of a "ring oscillator." The patent owner discussed features of a ring oscillator, such as being **non-controllable**, and being **variable based on the environment**. **The patent owner argued that these features distinguish over what Talbot teaches**. The examiner will reconsider the current rejection based on a forthcoming response, which will include arguments similar to what was discussed.[34]

In its post-interview submission, the patent owner reiterated the contention that the claim should be allowed because Talbot disclosed a "voltage-controlled oscillator" and not the "ring oscillator" disclosed in the claim:

> Further, Talbot does not teach, disclose, or suggest the ring oscillator recited in claim 4. The Examiner cited col. 3, ll. 26-36, and oscillator circuit 12 shown in FIG. 1 of Talbot as teaching the recited ring oscillator. Talbot discusses a voltage-controlled oscillator (VCO) 12, but does not teach or disclose a ring oscillator.[35]

During the course of these claim construction proceedings, the inventors have continued to maintain that Talbot was overcome during reexamination because it does not disclose a "ring oscillator."[36]

---

[33] An examiner's interview summary may serve as a basis for finding a prosecution disclaimer that narrows the claim scope. See, e.g., Rheox, Inc. v. Entact, Inc., 276 F.3d 1319, 1322 (Fed. Cir. 2002); Biovail Corp. Int'l v. Andrx Pharms., Inc., 239 F.3d 1297, 1302-04 (Fed. Cir. 2001).

[34] (See Chen Decl., Ex. 4, Ex Parte Reexamination Interview Summary, Docket Item No. 316-4 (emphasis added).)

[35] (Otteson Decl., Ex. Y, Remarks/Arguments at 11, hereafter, "Remarks," Docket Item No. 310-3.)

[36] For instance, Defendants argued during the Markman hearing that the inventors' written submission distinguished the Talbot reference because Talbot lacked a ring oscillator and never mentioned a requirement of "non-controllability." Further, Defendants also refer to the inventors' written response on February 21, 2008, which states:

> Further, **Talbot does not teach, disclose, or suggest the ring oscillator** recited in claim 4. ... Talbot discusses a voltage-controlled oscillator (VCO) 12, but **does not teach or disclose a ring oscillator**. Talbot provides two different implementations of the VCO 12 in FIGS. 3-4, **neither one of which is a ring oscillator**. Talbot refers to the oscillator of FIG. 3 as a "frequency controlled oscillator" (col. 7, ll. 21-22) and the oscillator of FIG. 4 simply as a "voltage controlled oscillator" (col. 8, ll. 59-65). As the sole inventor of the cited reference,

The Court has examined the Talbot patent. Although the component is, indeed, referred to as a "voltage-controlled oscillator," declarations and other extrinsic materials that have been tendered during the claim construction proceedings call into question the validity of the inventors' contention to the PTO and to this Court that the "ring oscillator" is different from the "voltage-controlled oscillator" disclosed in Talbot. On the one hand, the Court has received extrinsic evidence that the voltage-controlled oscillator disclosed in Talbot *is* a ring oscillator. On the other hand, arguments have been submitted claiming that the voltage-controlled oscillator of Talbot *is not* a ring oscillator.[37]

Under clear Federal Circuit law, a submission made by an inventor during reexamination is regarded as a disavowal only if the court finds that the allegedly disavowing statement is "so clear as to show reasonable clarity and deliberateness, and so unmistakable as to show unambiguous evidence of disclaimer." Omega Eng'g, Inc. v. Raytek Corp., 334 F.3d 1314, 1325 (Fed. Cir. 2003) (citations omitted).

Here, before arriving at a decision on the definition of the phrase "ring oscillator" in the context of the Talbot reference, the Court finds that it would benefit from further briefing. In the supplement briefs, the declarants shall fully articulate the technical basis for their opinions with respect to whether the voltage-controlled oscillator disclosed in Talbot is or is not a ring oscillator. The Court will return to the construction of the phrase "ring oscillator" following the completion of the supplement briefing.

> Talbot presumably possesses at least ordinary skill in the art, yet Talbot did not characterize either of the disclosed oscillators as ring oscillators. Applicants respectfully assert that the reason they were not characterized by Talbot as ring oscillators is because **they are not ring oscillators**. For at least the foregoing reasons, **Talbot does not teach, disclose, or suggest a ring oscillator** as recited in the claims. (Remarks at 11 (emphases added).)

[37] This issue is important to claim construction, because it is relevant to understanding in what manner the ring oscillator is "non-controllable," as distinguished from the voltage-controlled oscillator disclosed in Talbot. Resolving this conflict might affect how the Court approaches issues with respect to the validity of the patent claim at issue.

2. Claim 6

Claim 6 of the '336 Patent provides:

> A microprocessor system comprising:
> a central processing unit disposed upon an integrated circuit substrate, said central processing unit operating at a processing frequency and being constructed of a first plurality of electronic devices;
> an entire oscillator disposed upon said integrated circuit substrate and connected to said central processing unit, said oscillator **clocking said central processing unit** at a clock rate and being constructed of a second plurality of electronic devices, thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way **as a function of parameter variation** in one or more fabrication or operational parameters associated with said integrated circuit substrate, thereby enabling said processing frequency to track said clock rate in response to said parameter variation; an on-chip input/output interface, connected between said central processing unit and an off-chip external memory bus, for facilitating exchanging coupling control signals, addresses and data with said central processing unit; and
> an off-chip external clock, independent of said oscillator, connected to said input/output interface wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said oscillator and wherein a clock signal from said off-chip external clock originates from a source other than said oscillator.

a. "clocking said central processing unit"

The parties tender for construction the phrase "clocking said central processing unit."

Upon review, the Court finds that to one of ordinary skill in the art, the plain and ordinary meaning of "clocking said central processing unit" is to provide a clock signal to the central processing unit.

A further issue tendered with respect to this phrase is whether, based on the written description, the construction should include a limitation of the maximum or optimum frequency of the "clocking" function. In the written description of the '336 Patent, the phrase "maximum frequency possible" is used with respect to an embodiment.[38] A description of an embodiment in the specification may not be imposed as a limitation "unless the patentee has demonstrated a clear

[38] (See '336 Patent, Col. 16:67-17:2 (stating that "[b]y deriving system timing from the ring oscillator 430, CPU 70 will always execute at the maximum frequency possible, but never too fast.").)

intention to limit the claim scope using 'words or expressions of manifest exclusion or restriction.'" Innova/Pure Water, Inc. v. Safari Water Filtration Sys., Inc., 381 F.3d 1111, 1117 (Fed. Cir. 2004) (citation omitted). Here, the Court finds that the cited language does not demonstrate "a clear intention to limit the claim scope." Id.

Accordingly, the Court construes "clocking said central processing unit" to mean:

providing a timing signal to said central processing unit.

b. "as a function of parameter variation"

The parties tender for construction the phrase "as a function of parameter variation." The full phrase is: "thus varying the processing frequency of said first plurality of electronic devices and the clock rate of said second plurality of electronic devices in the same way **as a function of parameter variation."**

The disputed issue is whether the phrase requires a mathematical type predetermined functional relationship. Upon review, the Court finds that a person of ordinary skill in the art reading the patent would understand that the phrase "as a function of" is describing a variable that depends on and varies with another.[39] Because neither the written description nor the prosecution history provide a basis for concluding that the phrase should be limited to a narrower definition of an exact mathematical type functional relationship, the Court declines to do so. Having resolved the only dispute tendered with respect to this phrase, the Court declines to construe it further.

3. Claim 10

Claim 10 of the '336 Patent provides:

> In a microprocessor system including a central processing unit, a method for clocking said central processing unit comprising the steps of:
>
> providing said central processing unit upon an integrated circuit substrate, said central processing unit being constructed of a

[39] The Court observes that "function" is a very broad term. See, e.g., MODERN DICTIONARY OF ELECTRONICS 311-12 (7th ed. 1999) (defining "function" as, *inter alia*, a "quantity of value that depends on the value of one or more other quantities" or a "specific purpose of an entity, or its characteristic action," and defining a number of phrases that include the term "function," such as "function codes," "function keys" and a "function table").

> first plurality of transistors and being operative at a processing frequency;
>
> **providing an entire variable speed clock disposed upon said integrated circuit substrate**, said variable speed clock being constructed of a second plurality of transistors;
>
> clocking said central processing unit at a clock rate using said variable speed clock with said central processing unit being clocked by said variable speed clock at a variable frequency dependent upon variation in one or more fabrication or operational parameters associated with said integrated circuit substrate, said processing frequency and said clock rate varying in the same way relative to said variation in said one or more fabrication or operational parameters associated with said integrated circuit substrate;
>
> connecting an on-chip input/output interface between said central processing unit and an off-chip external memory bus, and exchanging coupling control signals, addresses and data between said input/output interface and said central processing unit; and
>
> clocking said input/output interface using an off-chip external clock wherein said off-chip external clock is operative at a frequency independent of a clock frequency of said variable speed clock and wherein a clock signal from said off-chip external clock originates from a source other than said variable speed clock.

The parties have tendered for construction the phrase "providing an entire variable speed clock disposed upon said integrated circuit substrate." There are two issues that are tendered with respect to this language. First, there is a dispute over whether the "variable speed clock" should be defined as limited to a ring oscillator. Here, the Court observes that, in other claims, the inventor discusses a "ring oscillator" as a variable speed system clock. Nonetheless, with respect to this Claim, the Court declines to limit the broader phrase found in Claim 10 to a ring oscillator only.

Second, the parties tender a dispute over the degree of independence between the signal of the "variable speed clock" and any external reference signal. However, upon review the Court finds that this dispute is not pertinent to the construction of the tendered phrase.

Accordingly, the Court construes "providing an entire variable speed clock disposed upon said integrated circuit substrate" to mean:

> **Providing a variable speed clock that is located entirely on the same semiconductor substrate as the central processing unit.**

4. Claim 11

Claim 11 of the '336 Patent provides:

> A microprocessor system, comprising a single integrated circuit including a central processing unit and an entire ring oscillator variable speed system clock in said single integrated circuit and connected to said central processing unit for clocking said central processing unit, said central processing unit and said ring oscillator variable speed system clock each including a plurality of electronic devices correspondingly constructed of the same process technology with corresponding manufacturing variations, a processing frequency capability of said central processing unit and a speed of said ring oscillator variable speed system clock varying together due to said manufacturing variations and due to at least operating voltage and temperature of said single integrated circuit; an on-chip input/output interface connected to exchange coupling control signals, addresses and data with said central processing unit; and a second clock independent of said ring oscillator variable speed system clock connected to said input/output interface, **wherein said central processing unit operates asynchronously to said input/output interface**.

The parties tender for construction the phrase "wherein said central processing unit operates asynchronously to said input/output interface."

Claim 11 discloses a microprocessor system comprising, among others, a central processing unit and an entire ring oscillator variable speed system clock connected to said central processing unit, an on-chip input/output interface, and "a second clock independent of said ring oscillator variable speed system clock" connected to said input/output interface. The subject phrase is contained in a "wherein" clause that describes the relationship between the timing control signal of the central processing unit and the timing signal of the on-chip input/output interface. The claim discloses that the central processing unit operates "asynchronously" to the input/output interface.

The written description is silent as to whether there is or can be *any* timing relationship between the central processing unit and the input/output interface or between their respective clocks.

The inventors first introduced the term "operates asynchronously to" during the re-examination of the '336 Patent in order to "clarify the meaning of 'independent' as recited in the

claims."[40] The examiner had focused on a reference known as "Kato" that purported to show two clock signals that are "in synchronism with each other." (Id. at 19.) The inventors explained that "Kato does not reveal any teaching that any of the components of the data processing circuit operate asynchronously with each other." (Id.) In support of the "independent" and "asynchronous" nature of its clocks, the inventors cited a textbook that describes what an asynchronous system is:

> An *asynchronous* system is one containing two or more independent clock signals. So long as each clock drives independent logic circuitry, such a system is effectively a collection of independent synchronous systems. **The logical combination of signals derived from independent clocks, however, poses difficulty because of the unpredictability of their phase relationship**.[41]

Reading this prosecution history, a person of ordinary skill would understand that the word "asynchronously"[42] means that the timing signal from one clock is independent from and not derived from the other clock such that a phase relationship between the two clocks is not readily predictable.

Accordingly, the Court construes "wherein said central processing unit operates asynchronously to said input/output interface" to mean:

> **the timing control of the central processing unit operates independently of and is not derived from the timing control of the input/output interface such that there is no readily predictable phase relationship between them.**

IV. CONCLUSION

The Court has construed the phrases and terms tendered for construction.

On or before **June 29, 2012**, the parties shall meet and confer and file a Joint Statement addressing the following issues:

---

[40] (See Declaration of Eugene Mar in Support of Defendants' Opening Claim Construction Brief, Ex. G, In re Ex Parte Reexamination of U.S. Patent No. 5,809,336 at 17, Docket Item No. 213-2.)

[41] (Id. (citing STEPHEN A. WARD & ROBERT H. HALSTEAD, JR., COMPUTATION STRUCTURES 93 (1990)) (emphasis added).)

[42] One source provides nine different meanings for the term "asychronous." See MODERN DICTIONARY OF ELECTRONICS 40 (7th ed. 1999) (defining the term, *inter alia*, as a "communication method in which data is sent when it is ready without being referenced to a timing clock, rather than waiting until the receiver signals that it is ready to receive" or as referring to "computer program execution [that is] unexpected or unpredictable with respect to the instruction sequence").

(1) A proposed schedule for supplemental briefs consistent with the terms of this Order;

(2) In light of the Court's impending retirement,[43] the Court proposes to assign this case to Magistrate Judge Grewal. In their Statement, the parties shall state whether they jointly consent to having this case immediately reassigned to Judge Grewal. In the event the parties do not consent to the immediate reassignment, the case will remain with Judge Ware and be subject to reassignment in due course.

Dated: June 12, 2012

JAMES WARE
United States District Chief Judge

[43] On April 28, 2012, Chief Judge Ware announced that he plans to "retire in August 2012 as the terms of his current law clerks come to an end." See Chief Judge Ware Announces Transition, *available at* http://www.cand.uscourts.gov/news/82.

THIS IS TO CERTIFY THAT COPIES OF THIS ORDER HAVE BEEN DELIVERED TO:

Deepak Gupta dgupta@fbm.com
Eugene Y. Mar emar@fbm.com
Harold H. Davis harold.davis@klgates.com
James Carl Otteson jim@agilityiplaw.com
Jas S Dhillon jas.dhillon@klgates.com
Jeffrey M. Fisher jfisher@fbm.com
Jeffrey Michael Ratinoff jeffrey.ratinoff@klgates.com
John L. Cooper jcooper@fbm.com
Kyle Dakai Chen kyle.chen@cooley.com
Mark R. Weinstein mweinstein@cooley.com
Michelle Gail Breit mbreit@agilityiplaw.com
Nan E. Joesten njoesten@fbm.com
Paul A. Alsdorf palsdorf@fbm.com
Samuel Citron O'Rourke eupton@whitecase.com
Stephanie Powers Skaff sskaff@fbm.com
Timothy Paar Walker timothy.walker@klgates.com
William Sloan Coats william.coats@kayescholer.com

Dated: June 12, 2012

Richard W. Wieking, Clerk

By: /s/ JW Chambers
William Noble
Courtroom Deputy